

Vertex Detector R&D for CLIC



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on behalf of the CLICdp collaboration

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CLIC - a collider for the future



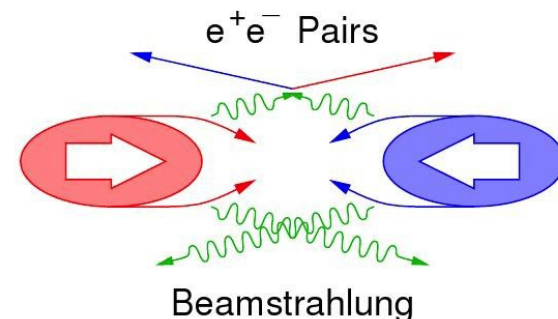
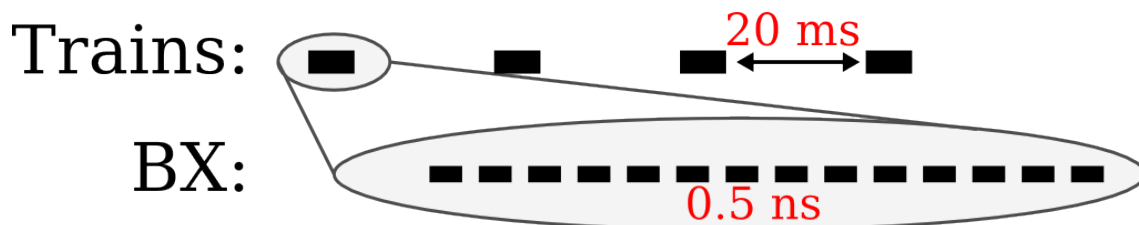
CLIC: concept for e^+e^- linear collider with \sqrt{s} up to 3 TeV, aiming at performing precision measurements of Standard Model (Higgs, top) and seeking new physics beyond Standard Model

... its program is complementary to LHC

More details presented by Lucie, Sophie, Steinar

Challenging machine environment:

- Beam profile: **45 nm / 1 nm / 44 μm** ($\sigma_x / \sigma_y / \sigma_z$)
→ Beamstrahlung creates high particle rate 'beam induced backgrounds'
- Time beam structure:
 - Bunch crossing separation : **0.5 ns**
 - Bunches per train : 312 (**156 ns**)
 - Repetition rate : 50 Hz

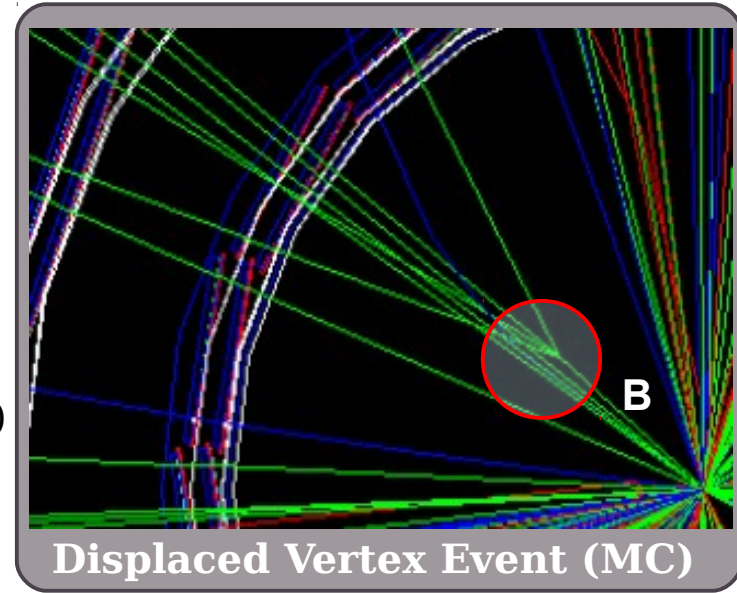


Drives timing requirements for CLIC detectors

Vertex Detector Requirements



- Efficient tagging of heavy quarks
(through precise determination of displaced vertices)
- good single point resolution: $\sigma_{SP} \sim 3 \mu\text{m}$
→ small pixels $< \sim 25 \times 25 \mu\text{m}^2$ (analog readout)
- low material budget: $X \lesssim 0.2\% X_0 / \text{layer}$
(corresponds to $\sim 200 \mu\text{m}$ Si, including supports, cables, cooling)
→ very thin sensors and ASIC ($\sim 50 + 50 \mu\text{m}$)
→ gas-flow cooling
→ low-power ASICs ($\sim 50 \text{ mW/cm}^2$)
- 156 ns bunch trains
→ **trigger-less readout**
- 20 ms gaps between trains
→ **power pulsing**
- Beam-induced background
→ **time stamping $\sim 10 \text{ ns}$**
- Moderate radiation exposure
($\text{NIEL} < 10^{11} \text{ n}_{\text{eq}}/\text{cm}^2/\text{y}$, $\text{TID} < 200 \text{ Gy} / \text{year}$)



Displaced Vertex Event (MC)



Multi-layer barrel and endcap pixel detectors
(560 mm in length, Barrel radius from 30 mm to ~ 70 mm)



Detector R&D road map



Motivation: Evaluate **performances and yield** of thin pixel sensor and demonstrate the feasibility of a good tracking efficiency with **thin assemblies**

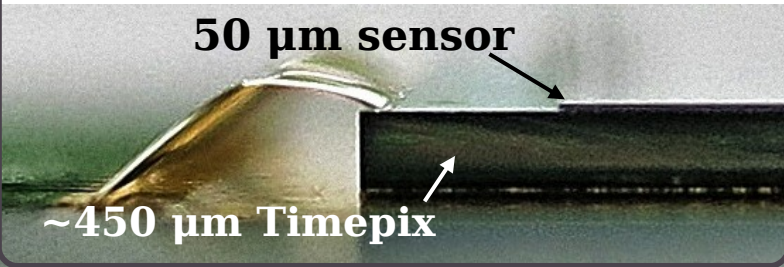
Ultimate goal: **50 μm** thick sensors + **50 μm** thick ASICs, **25 μm** pixel pitch

- **Timepix readout ASIC** ($55 \times 55 \mu\text{m}^2$ pixel pitch) was used for **feasibility tests** of ultra-thin sensors-assemblies (**50, 100, 200 μm** thick sensor on 450 μm and **100 μm** thick ASIC)
- **CLICpix** readout ASIC development (**25x25 μm^2** pixels). Assemblies with planar sensor in production (bump bonding challenging). Assemblies with **capacitively coupled HVCMOS active sensor** used to validate the chip.

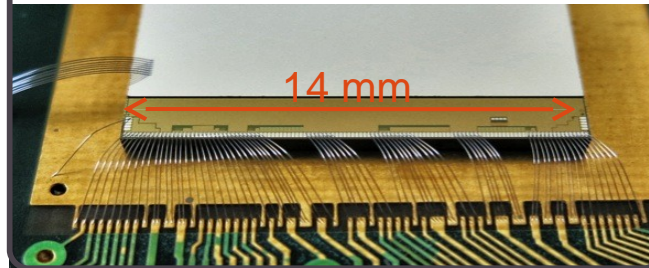


Thin sensor assemblies: laboratory tests

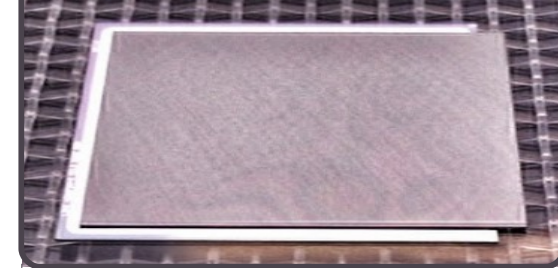
50 μm active-edge sensor (side view)



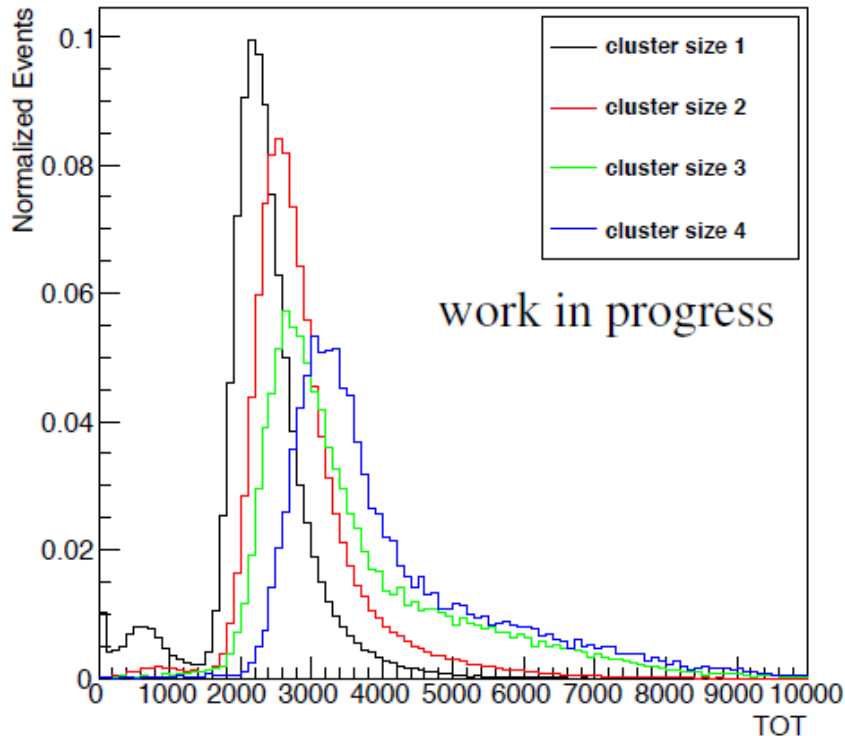
50 μm active-edge sensor (front view)



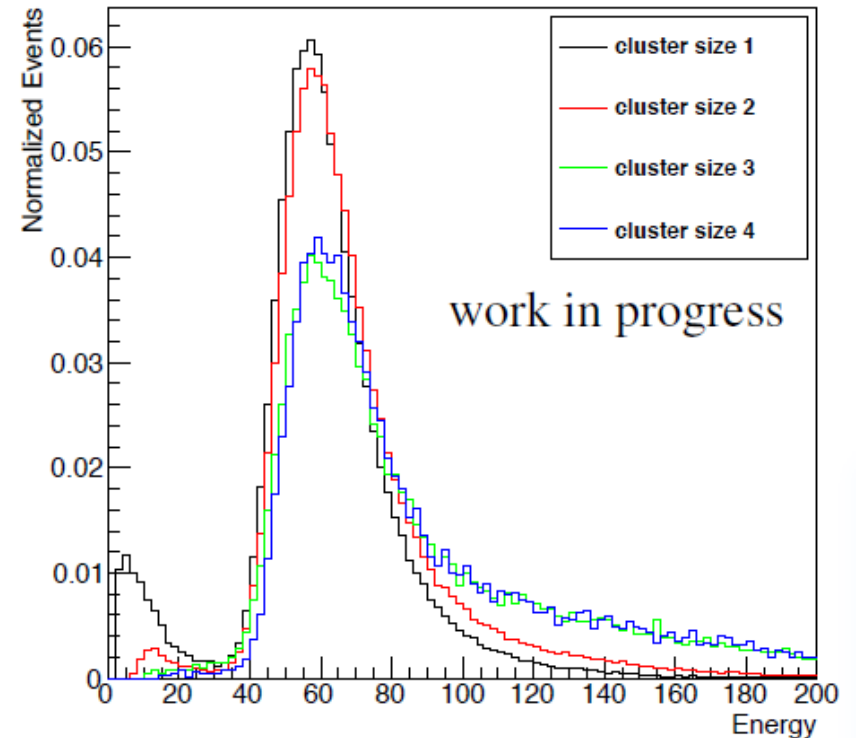
100 μm slim-edge sensor on 100 μm Timepix ASIC



Uncalibrated energy spectra



Calibrated energy spectra



200 μm thick sensor | sensor calibration was performed in lab tests at CERN and LNL S synchrotron. | Spectra for MIPs

Test beams at DESY and CERN

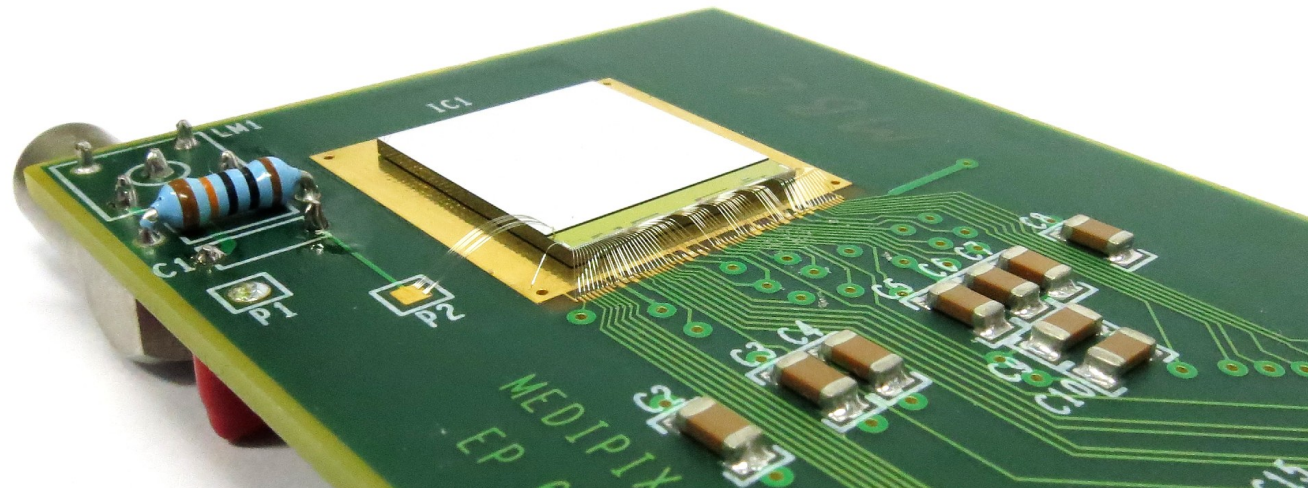
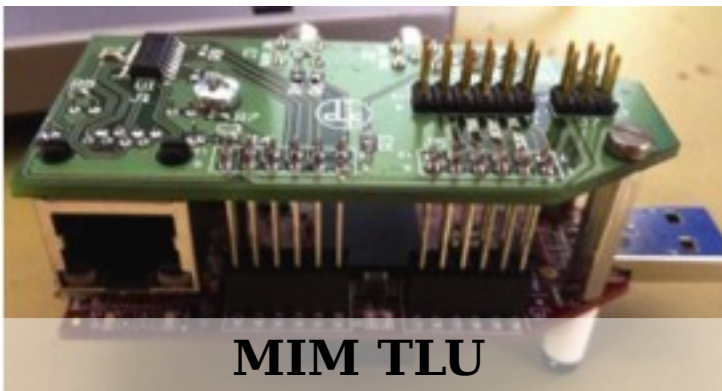
- **EUDET Telescope** based on MIMOSA detectors → resolution at DUT $\sim 3 \mu\text{m}$
- **Hardware and software integration** of Timepix detector (MIM TLU) with EUDAQ
- **Optimized** telescope **geometry**
- Assemblies on translational and rotational stages
- **Analysis software**



Telescope planes

DUT

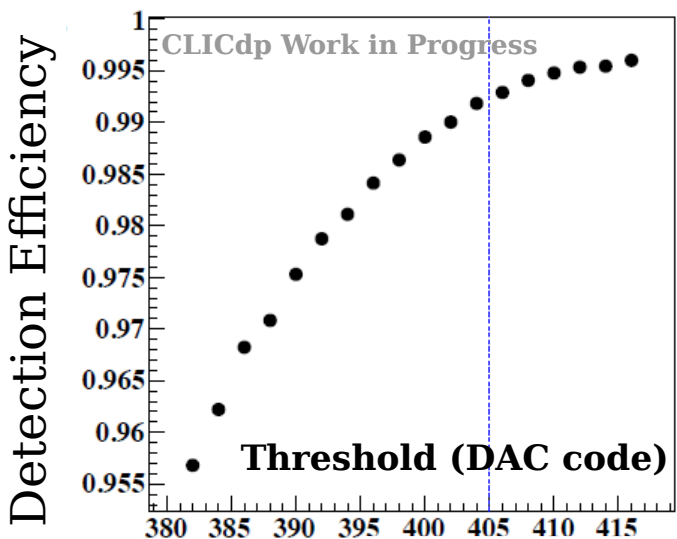
X/Y/ ϕ stage



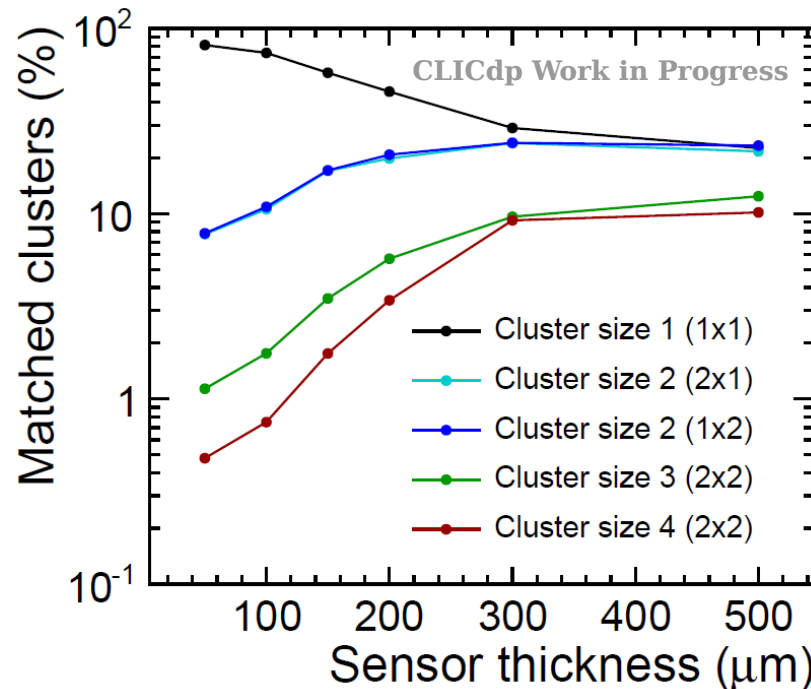
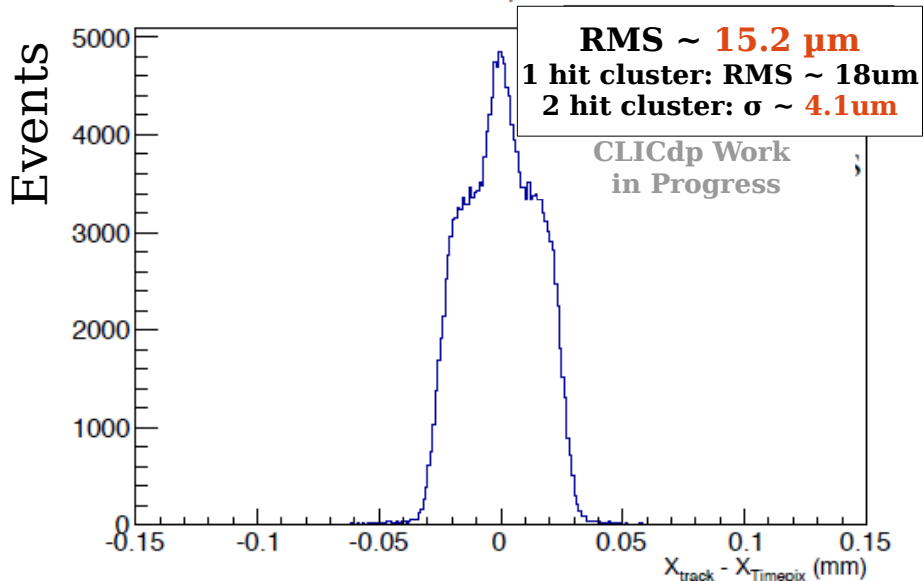
Thin sensor assemblies: testbeam results



50 μm thick p-in-n sensor assembly



Unbiased residual X, all clusters



Using **charge sharing information** (for cluster size > 1) it is possible to **gain more than factor of 3 in single-point resolution.**

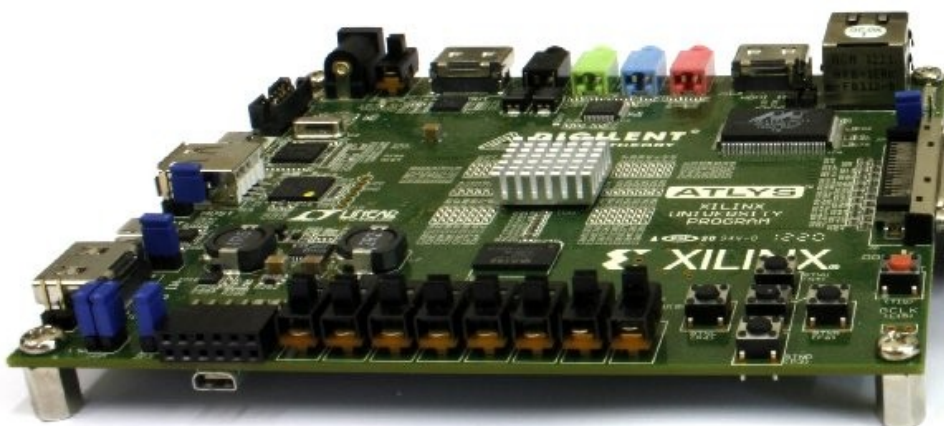
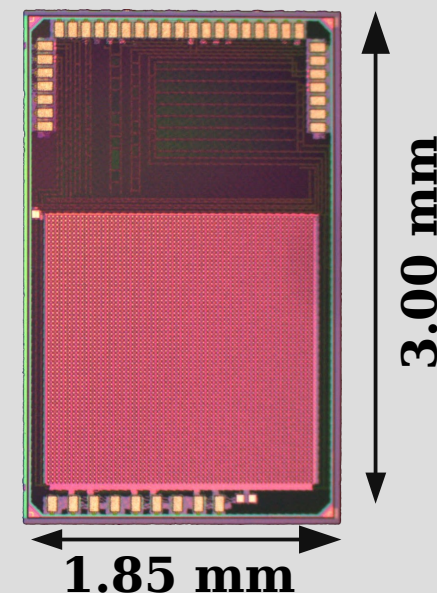
For **50 μm** thick sensor (and 55 μm pixel size) this type of events represents only 20% of the data \rightarrow **smaller pixel size is needed.**

CLICpix Chip and Readout system

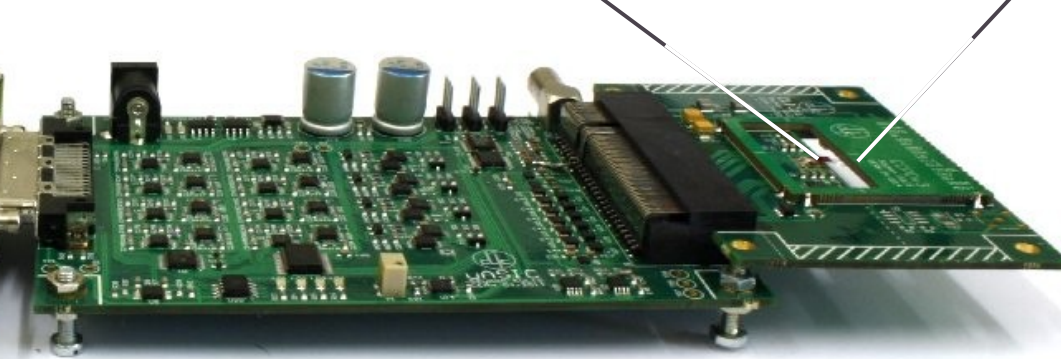


- **65 nm CMOS** hybrid r/o chip, targeted to CLIC vertex detectors
- based on Timepix/Medipix chip family, synergy with HL-LHC pixel r/o projects (RD53 collaboration on 65 nm r/o)
- demonstrator chip with **64 x 64 matrix**
- **25 μm pixel pitch**
- **simultaneous time** (4-bit TOA, 10ns) and **energy** (4-bit TOT) measurement per pixel
- selectable **compression logic** (pixel, cluster + column-based)
- power pulsing enabled ($P_{\text{avg}} < 50 \text{ mW/cm}^2$)

CLICpix
(64x64 pixels)



FPGA Board



Interface Board

Chip Board

Capacitively Coupled Pixel Detector



Conventional sensors require (costly and low pitch) bump-bonding in order to DC-couple the pixel implant with the amplifier input

- AC-coupling not previously used due to low coupling capacitance
- Can be overcome by amplification and shaping of the signal on the sensor side

Half way between conventional hybrid pixel detectors and fully-integrated CMOS circuits

Advantages:

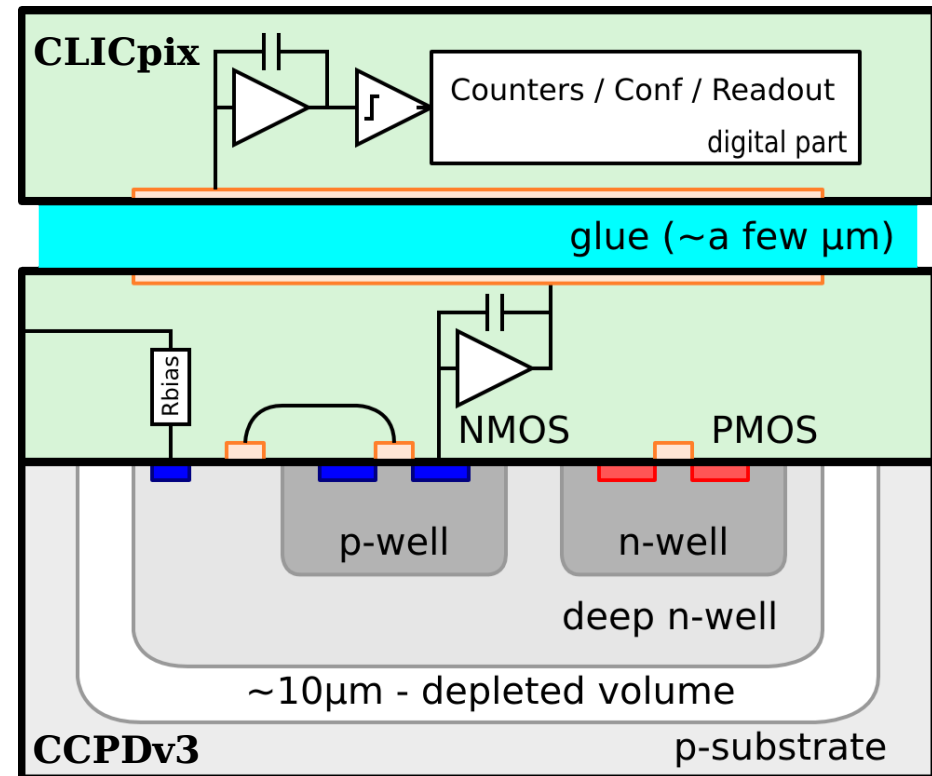
- low material budget (sensor can be thinned, active area is in order of $\sim 10\mu\text{m}$)
- sub pixels position encoding possible \rightarrow to a demonstrated
- industry standard deep n-well technology (large volume, cheap)
- cost savings (lack of bump-bonding) \rightarrow to a demonstrated

Disadvantages:

- sensor consumes power (may be significant)

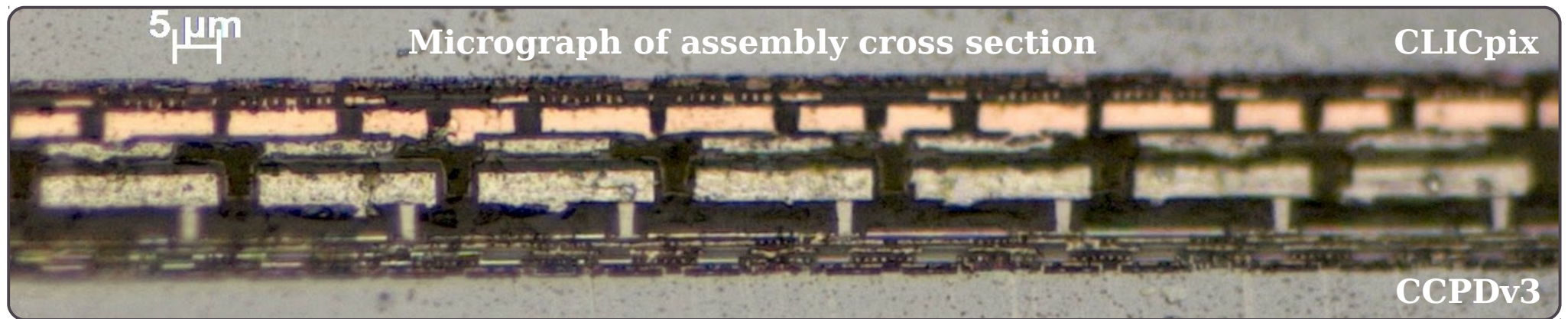
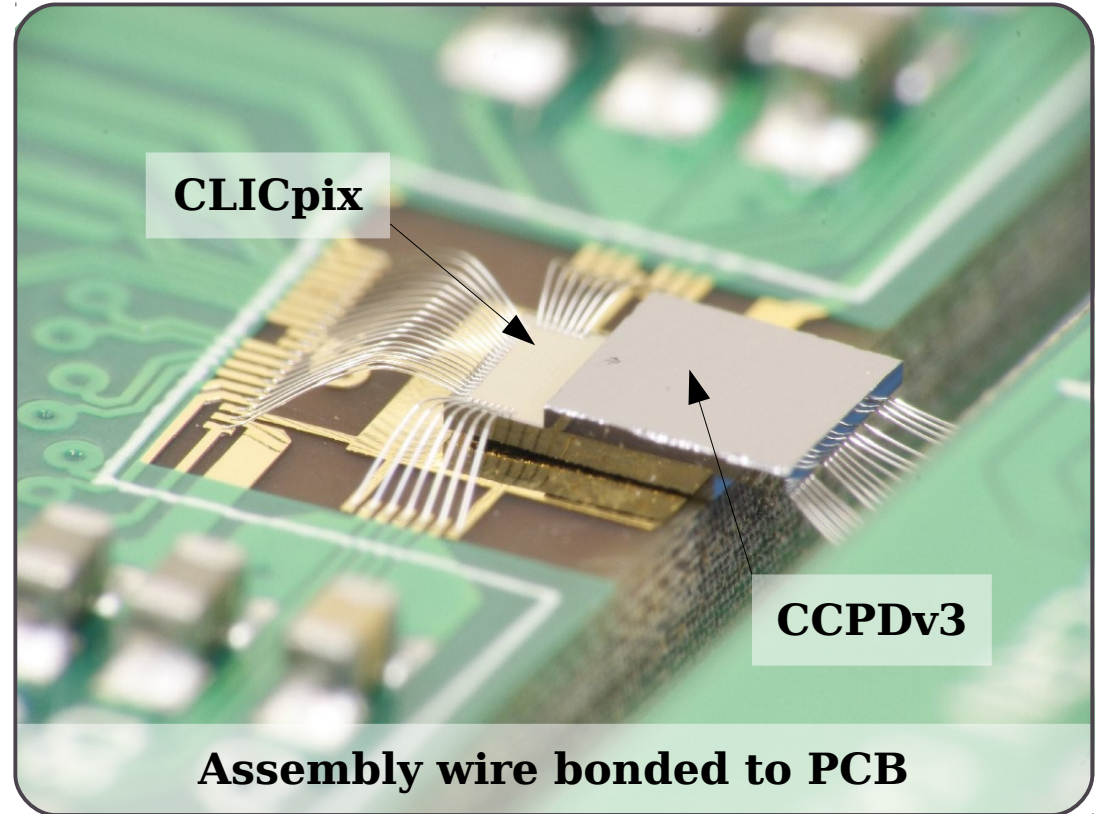
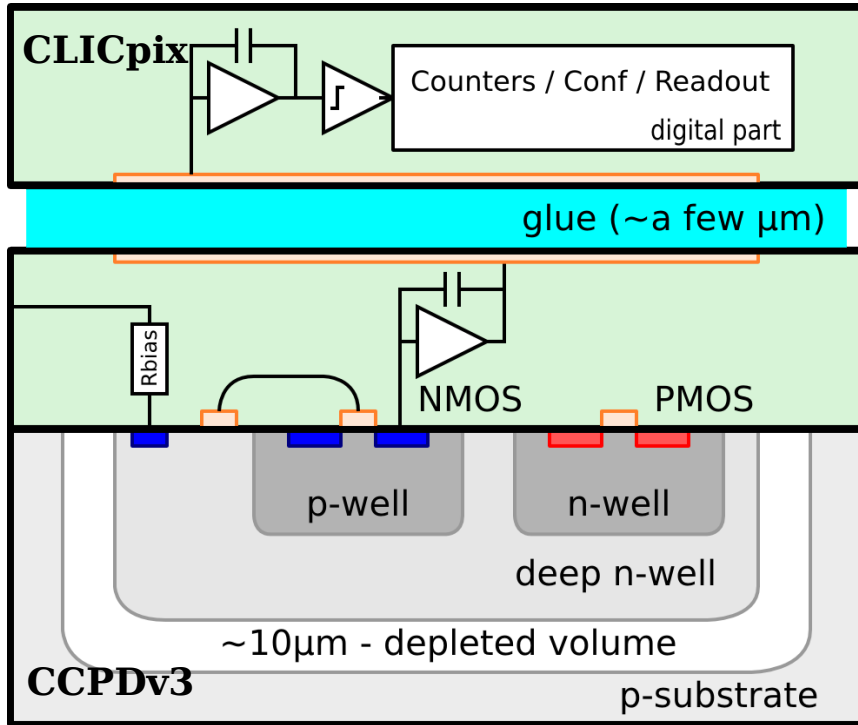
Challenges:

- precise gluing and alignment

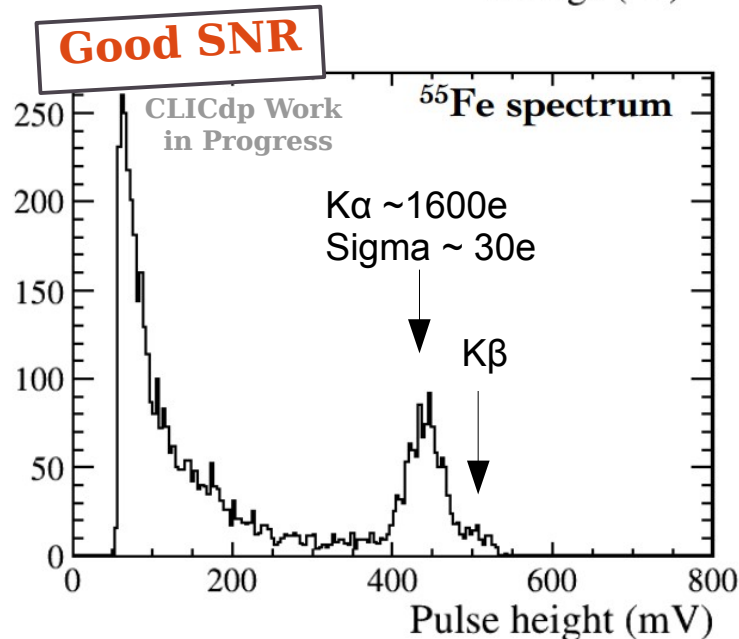
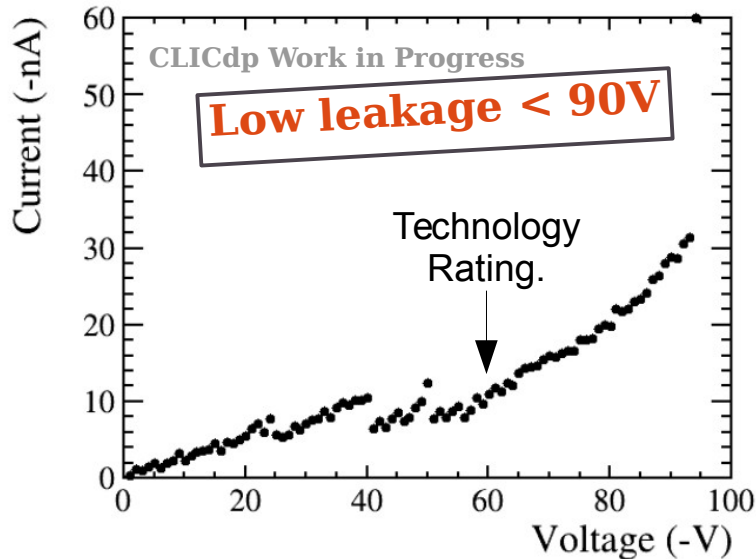




CCPD Assemblies



CCPDv3 only measurements

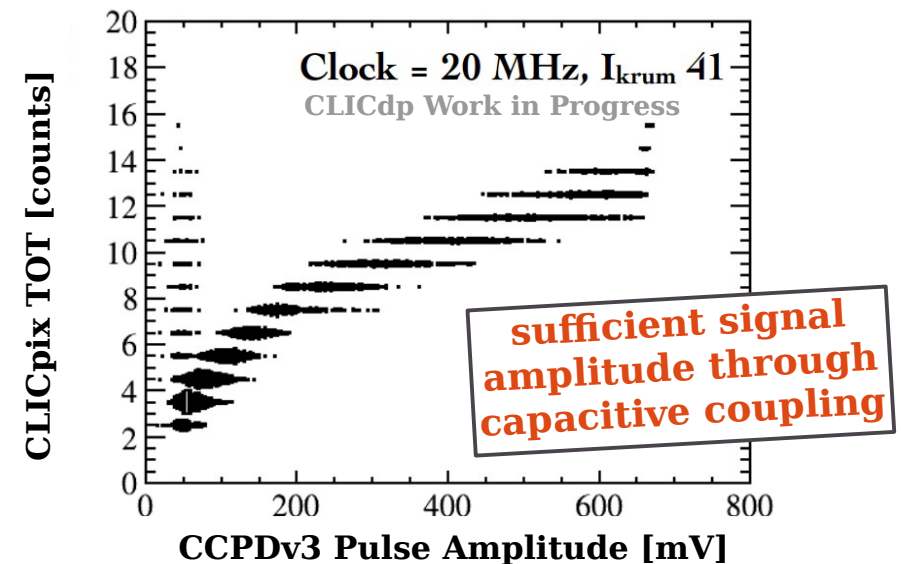


CLICpix performance

Chip has been fully characterized, nominal operating point:

- ENC: **55 [e-]** (without sensor)
- Threshold spread **128 / 22 [e-]** (uncalibrated/ calibrated)
- Power consumption: **7 [μW/pixel]** (without power pulsing)
- Gain: **44 [mV/ke]**
- Timing accuracy: **<10ns** (chip can be tuned to CCPD signals)

CLICpix + CCPD - coupling

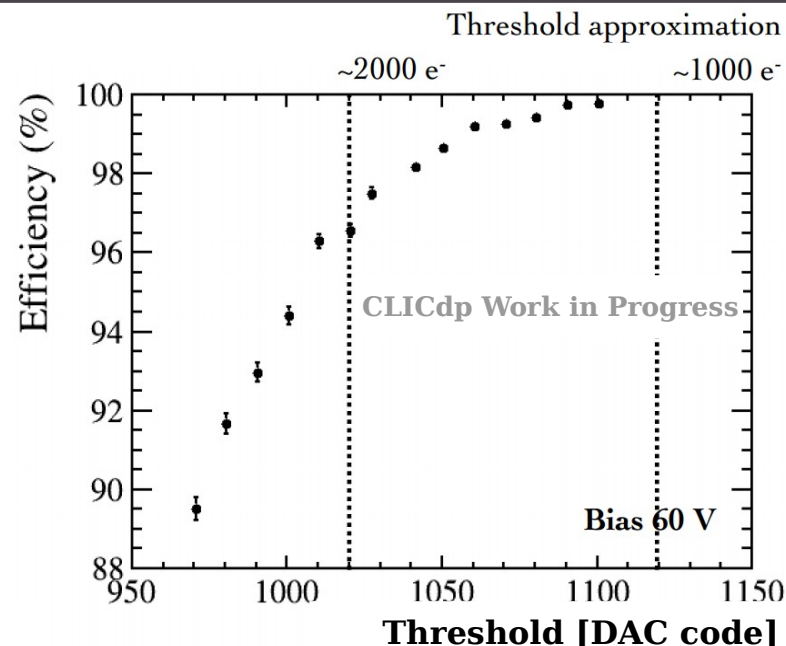
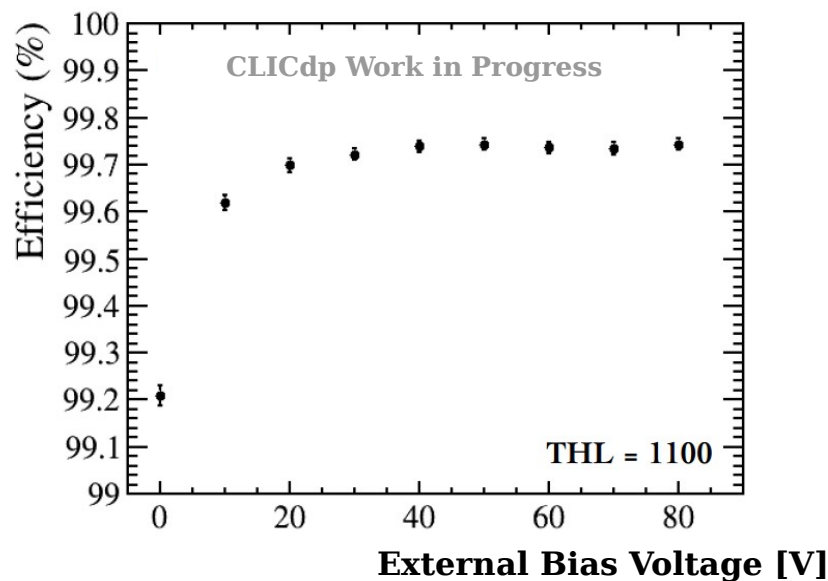




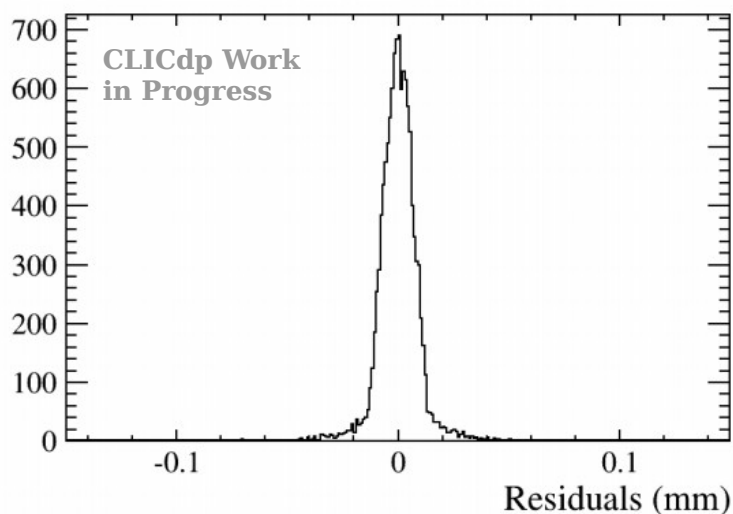
CLICpix & CCPDv3 - results



Detection efficiency



Residuals



Promising early results from CCPDv3 assemblies:

- **full matrix appears responsive**
- **high detection efficiency**
(even without applied bias voltage)

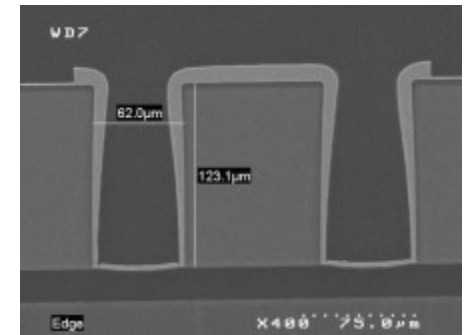
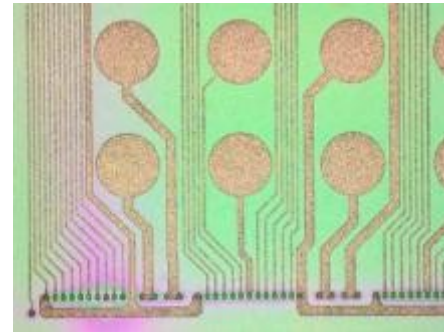
More studies needed to make device manufacture robust (gluing and measurements of the coupling capacitance)

Through-Silicon Vias (TSV)

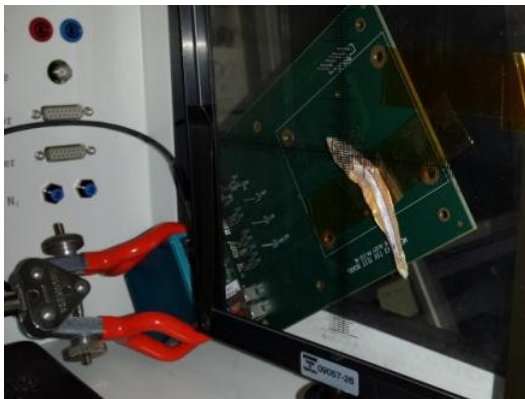


Through Silicon Via: **vertical electrical connection** passing through Si wafer

- eliminates need for wirebonds
- enables 4-side buttable chips
- increased reliability



Medipix3 redistribution layer SEM cross section of TSVs



X-ray setup



X-ray photograph

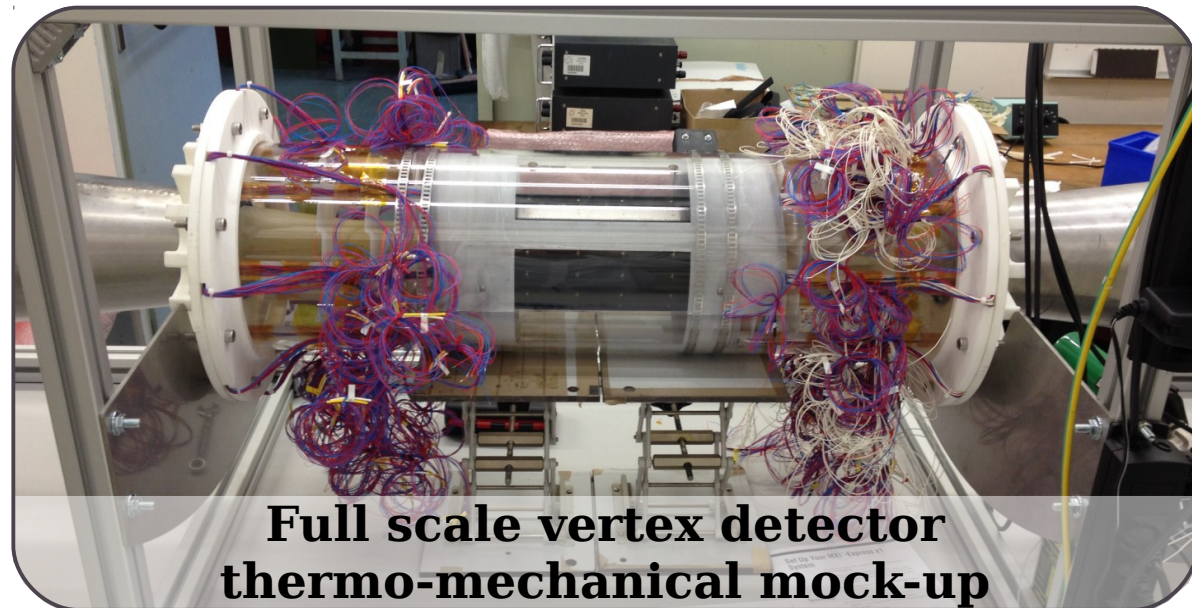
TSV project (ALICE, CLIC, ACEOLE, AIDA) with CEA-Leti

- 130 nm Medipix3 and Timepix3 wafers
- first phase: **feasibility demonstrated**
- second phase: **good yield demonstrated**
- on-going third phase:
TSV with 50 µm thick wafers (CLIC goal!)

500 µm sensor on 120 µm ASIC bump bonded to PCB (side view)



- Evaluation of forced convection air cooling (*full scale prototype*)
- Measurement & characterization air-flow induced vibrations (*wind tunnel, laser sensor*)
- Development and characterization of low-mass ladder support ($\sim 0.05\% X_0$)



Ladder support structure prototypes





Summary & Outlook



- CLIC environment + physics requirements pose challenging demands on vertex-detector system (*a new kind of challenges compared to LHC*)
 - Less radiation damage but ...
 - Higher spatial resolution precision ($\sim 3 \mu\text{m}$)
 - Finer time stamping ($\sim 10 \text{ ns}$)
 - Lower power ($0.3 \mu\text{W}/\text{channel}$, $50 \text{ mW}/\text{cm}^2$)
 - Lower material budget ($0.2 \% X_0$)
- Ongoing active R&D on:
 - Thin sensors
 - Readout technologies
 - Interconnection technologies
 - Power-delivery and power pulsing (*not covered in this talk*)
 - Mechanics, cooling

